

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 01-196148

(43)Date of publication of application : 07.08.1989

(51)Int.Cl.

H01L 21/92

H01L 21/60

(21)Application number : 63-019482

(71)Applicant : MATSUSHITA ELECTRON CORP

(22)Date of filing : 01.02.1988

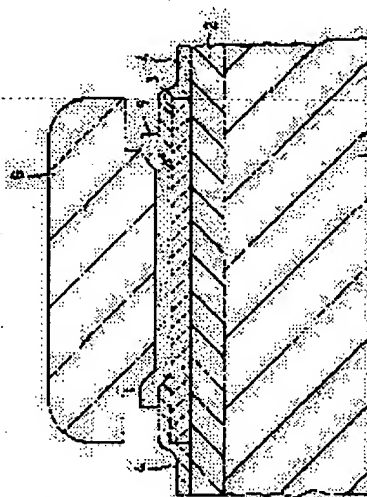
(72)Inventor : YAMAOKA TORU

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To enhance a pressurization limit of a pressure to be exerted on a semiconductor chip during an ILB(inner lead bonding) process as one of mounting processes of the semiconductor chip having a bump by a method wherein a cross-sectional shape of a surface protective film on an aluminum pad is formed to be a sloped shape whose taper angle is specified.

CONSTITUTION: When a silicon nitride film as a surface protective film is to be treated, a resist baking operation is executed prior to a dry etching process; the shape of a resist is controlled, an etching rate of the dry etching process is lowered, or the like; the shape to be etched of the silicon nitride film 4 is formed to be a sloped shape whose taper angle is 70° or below. By constituting this structure, it is possible to relax the concentration of a stress in the transverse direction at an end part of an aluminum pad 3 due to a pressure to be exerted on a bump 6 during an ILB process and to enhance a pressurization limit during the ILB process. When the shape to be etched of the silicon nitride film 4 is formed to be a sloped shape with a taper angle of 70° or below, there occurs no problem even when the pressure to be exerted on the bump 6 during the ILB process is increased to 1t/cm² or more.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office

JAPANESE LAID-OPEN PATENT APPLICATION

H1-196148 (1989)

| | | |
|--|-----------------------|-------------------------|
| (19) Japan Patent Office (JP) | (11) Publication No. | H1-196148 |
| (12) Published Unexamined Patent Application (A) | (43) Publication Date | August 7, 1989 |
| (51) Int. Cl. ⁴ | Identification Code | In-House Reference. No. |
| H 01 L 21/92 | | C-6708-5F |
| 21/60 | | Q-6918-5F |

No examination request

Number of claims 1 (totally 3 pages)

(54) Title of the Invention

SEMICONDUCTOR DEVICE

| | |
|----------------------|--|
| (21) Application No. | PA S63-19482 |
| (22) Date of Filing | February 1, 1988 (Showa 63) |
| (72) Inventor | Toru YAMAOKA c/o Matsushita Electron Corp. 1006 Oaza Kadoma Kadoma-shi, Osaka |
| (71) Applicant | c/o Matsushita Electron Corp. 1006 Oaza Kadoma Kadoma-shi, Osaka Japan |

(74) Agent

Satoshi Hoshino, Attorney

Specification

Title of the Invention

Semiconductor Device

Scope of Claims

Claim 1

A semiconductor device, wherein the cross-sectional shape of the surface protective coat on an aluminum pad is a slope where the taper angle is 70° or below in a construction where the use of a bump is one of the mounting methods of a semiconductor chip.

Description of the Invention

Industrial Applications

The present invention relates to a semiconductor device designed to enhance the critical value of the pressure applied at the time of mounting relative to a semiconductor chip having a bump.

Prior Art

As a result of demand in recent years for the miniaturization of electronic devices, bump technology has been focused on as a mounting technology for semiconductor chips. Fig. 2 illustrates an example of conventional bump construction and its manufacturing method. In the drawing, the field oxide

film 2 having a 1 to 2 μm thickness is formed on a silicon substrate 1, and the aluminum pad 3 is formed thereon. Subsequently, the silicon nitride film 4 is formed on the aluminum pad 3 as a surface protective coat, and the silicon nitride film 4 on the aluminum pad 3 is removed selectively by using dry etching. At this time, the etching shape of the silicon nitride film 4 is larger than the taper angle 70° , and the shape is nearly perpendicular, even though isotropy dry etching is used because over etching has been performed in order to stabilize the contact adhesive performance with the aluminum pad 3 at the time of normal etching. Then, a barrier metal 5 is formed by selectively forming titanium, palladium, or so forth on the aluminum pad 3. Thereafter, bump construction can be obtained by making the bump 6 grow selectively by about 10 to 20 μm by using a method such as plating, with gold or the like.

Problems overcome by the invention

At the time of the ILB (Inner Lead Bonding) that is one of the mounting processes of a semiconductor chip having a bump in conventional bump construction as described above, when a pressure of 1 (t/cm^2) or above is applied at a temperature of 300 to 500 $^\circ\text{C}$, the force is spread sideways through the aluminum pad, causing cracks in the silicon nitride film at the edge of the aluminum pad according to the stress. This leads to problems with the reliability of the semiconductor device, with the problem that the pressure added in order to adhere the bump and the lead material at the time of the ILB processing is limited.

The object of the present invention is to overcome existing weaknesses and to provide a semiconductor device that has the ability to enhance the pressurization limit of the pressure added to the semiconductor chip by ILB processing, which is one of the methods of mounting processing of a semiconductor chip having a bump.

Problem resolution means

A semiconductor device according to the present invention comprises a cross-sectional shape of the

surface protective coat on an aluminum pad which has a sloped shape where the taper angle is 70° or below in a construction where a bump is one of the mounting method of a semiconductor chip.

Operation

Although the applied pressure has been restricted in the upper limit with the conventional bump construction as described above, ILB processing can be performed easily at a higher pressure, and mounting having high reliability and stability can be made possible.

Embodiments

An Embodiment according to the present invention is provided hereafter, with reference to Fig. 1. Fig. 1 is a cross-sectional view of the bump construction of the semiconductor according to the present invention. In the drawing, the same numerals are given in the same sections with the conventional side illustrated in Fig. 2, and the description will be omitted.

In comparison with the conventional example shown in Fig. 2, there are no differences fundamentally in the materials and the manufacturing processes in order to form the bump. However, when the silicon nitride film comprising the surface protective coat is processed, the etching shape of the silicon nitride film 4 is made to be a sloped shape where the taper angle is 70° or below, as illustrated in Fig. 1, by controlling the resist shape by performing resist baking before the dry etching process, and also by lowering the etching rate of the dry etching and the like. By making such a construction, the stress concentration in the lateral direction on the edges of the aluminum pad 8, which occurs due to the applied pressure against bump 6 at the time of the ILB processing, can be relieved, and the pressurization limit at the time of ILB processing can be enhanced. In the construction of the conventional side illustrated in Fig. 2, there is the problem in mounting of such as cracks in the silicon nitride film 4 in the vicinity of the edge of the aluminum pad 3 and so forth, due to the stress concentration in the lateral direction that occurs at the edge of the aluminum pad 3, when the pressure applied to the bump 6 is 1 (t/c) or above at the time of the ILB processing. However, as

illustrated in Fig. 1, by making the etching shape of the silicon nitride film 4 to be a sloped shape where the taper angle is 70° or below, the problem will not occur, even if the pressure applied to the bump 6 is $1 \text{ (t/cm}^2\text{)}$ or above at the time of the ILB processing.

Efficacy of the Invention

According to the present invention, the pressurization limit can be enhanced for pressure applied to a semiconductor chip in ILB processing comprising one of the mounting methods of a semiconductor chip with a bump, and mounting having a high reliability and stability can be made possible, with significant efficacy in practical use.

Brief Description of Drawings

Fig. 1 is a cross-sectional view of a semiconductor device according to the Embodiment of the present invention, and Fig. 2 is a cross sectional view of the conventional semiconductor device.

- 1 Silicon substrate
- 2 Field oxide film
- 3 Aluminum pad
- 4 Silicon nitride film
- 5 Barrier metal
- 6 Bump

Applicant: Matsushita Electronics

Agent: Satoshi Hoshino

⑨ 日本国特許庁(JP)

⑩ 特許出願公開

⑫ 公開特許公報(A) 平1-196148

⑬ Int.Cl.⁴

H 01 L 21/92
21/60

識別記号

庁内整理番号

C-6708-5F
Q-6918-5F

⑭ 公開 平成1年(1989)8月7日

審査請求 未請求 請求項の数 1 (全3頁)

⑮ 発明の名称 半導体装置

⑯ 特 願 昭63-19482

⑰ 出 願 昭63(1988)2月1日

⑱ 発 明 者 山 岡 徹 大阪府門真市大字門真1006番地 松下電子工業株式会社内
⑲ 出 願 人 松下電子工業株式会社 大阪府門真市大字門真1006番地
⑳ 代 理 人 弁理士 星野 恒司

明 細 書

1. 発明の名称 半導体装置

2. 特許請求の範囲

半導体チップの実装手段の一つであるバンプの構造において、アルミパッド上の表面保護膜の断面形状がテーパ角度70°以下のスロープ状であることを特徴とする半導体装置。

3. 発明の詳細な説明

(産業上の利用分野)

本発明は、バンプ付半導体チップに対して実装時に加わる圧力の限界値の向上を図った半導体装置に関するものである。

(従来の技術)

近年、電子機器の小型化が要求される中にあって、半導体チップの実装技術としてバンプ技術が注目されている。従来のバンプ構造とその製造方法の一例を第2図に示す。同図において、シリコン基板1の上に厚さ1～2μmのいわゆるフィールド酸化膜2が形成され、その上にアルミパッド3

が形成されている。アルミパッド3の上に表面保護膜としてシリコン窒化膜4を形成したのち、アルミパッド3上のシリコン窒化膜4をドライエッチングを用いて選択的に除去する。この際、通常エッチング時にはアルミパッド3とのコンタクト性を安定にするため、オーバーエッチングが行われるため、等方性のドライエッチング装置を用いても、シリコン窒化膜4のエッチング形状はそのテーパ角度が70°よりも大きく、垂直に近い切り立った形状になっている。こののちに、チタンまたはパラジウムなどをアルミパッド3上に選択的に形成し、バリアメタル5を形成する。そののちに、金などをメッキなどの方法を用いて10～20μm程度選択的にバンプ6を成長させることによりバンプ構造が得られる。

(発明が解決しようとする課題)

上記、従来のバンプ構造では、バンプ付半導体チップ実装工程の一つであるILB(Inner Lead Bonding)工程時に、バンプに300～500℃の温度で1(t/cd)以上の圧力が加わった場合、その力が

アルミパッドを通して横方向に広がり、その応力によりアルミパッド端部でシリコン窒化膜にクラックが生じ、半導体デバイスの信頼性上問題となるため、ILB工程時にパンプとリード材料を接合するために加える圧力が制限される欠点があった。

本発明の目的は、従来の欠点を解消し、パンプ付半導体チップの実装工程の一つであるILB工程で半導体チップに加える圧力の加圧限界を向上させることができる半導体装置を提供することである。

(問題を解決するための手段)

本発明の半導体装置は、半導体チップの実装手段の一つであるパンプの構造において、アルミパッド上の表面保護膜の断面形状がテーパ角度70°以下のスロープ状とするものである。

(作用)

上記構成により、従来のパンプ構造では、ILB工程時に加える圧力の上限に制限を受けていたものが、より高い圧力でILB工程を実施するこ

とが容易となり、信頼性の高い安定した実装を行うことが可能となる。

(実施例)

本発明の一実施例を第1図に基づいて説明する。第1図は、本発明の半導体装置のパンプ構造の断面図である。同図において、第2図に示した従来例と同じ部分については同一符号を付し、その説明を省略する。

パンプを形成するための製造工程および材料は、第2図に示した従来例と基本的には相違ないが、表面保護膜であるシリコン窒化膜を加工する際、ドライエッチング工程の前にレジストベークングを行い、レジスト形状を制御し、かつドライエッチングのエッチングレートを低くする等の工夫をし、シリコン窒化膜4のエッチング形状を、第1図に示すようにテーパ角度70°以下のスロープ状にする。こういう構造にすることにより、ILB工程時にパンプ6に加わる圧力のために生じるアルミパッド3の端部の横方向の応力集中を緩和することができ、ILB工程時の加圧限界を向上

- 3 -

させることができる。第2図に示した従来例の構造では、ILB工程時にパンプ6に加わる圧力を1(t/cm²)以上にすると、アルミパッド3の端部に生じる横方向の応力集中のためにアルミパッド3の端部付近でシリコン窒化膜4にクラックが生じるなど実装上問題があったものが、第1図に示すように、シリコン窒化膜4のエッチング形状をテーパ角度70°以下のスロープ状にすることにより、ILB工程時にパンプ6に加わる圧力を1(t/cm²)以上にしても問題は生じない。

(発明の効果)

本発明によれば、パンプ付半導体チップの実装工程の一つであるILB工程で半導体チップに加える圧力の加圧限界を向上させることができ、信頼性の高い安定した実装が可能となり、その実用上の効果は大である。

4. 図面の簡単な説明

第1図は本発明の一実施例による半導体装置の断面図、第2図は従来の半導体装置の断面図である。

- 4 -

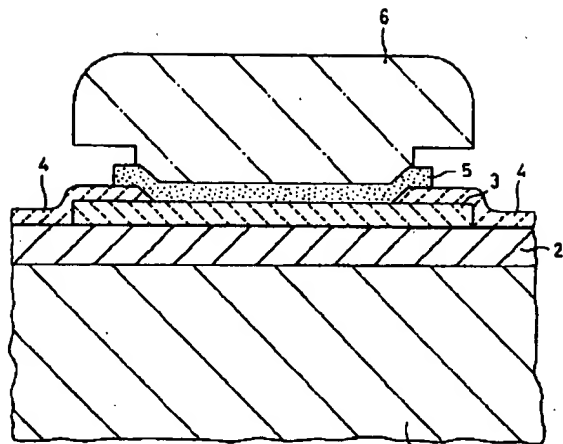
1…シリコン基板、 2…フィールド酸化膜、 3…アルミパッド、 4…シリコン窒化膜、 5…バリアメタル、 6…パンプ。

特許出願人 松下電子工業株式会社

代理人 星 野 恒



第 1 図



- 1... シリコン基根
- 2... フィールド酸化膜
- 3... アルミバッド
- 4... シリコン窒化膜
- 5... バリアメタル
- 6... ゲート

第 2 図

